NEW UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

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Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

MAGNETIC SHIELDING FOR INTEGRATED CIRCUITS

and invented by:

Mark Tuttle

IF A CONTINUATION APPLICATION, check appropriate box and supply requisite information:

☐ Continuation ☐ Divisional

☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. [X] Filing fee as calculated and transmitted as described below
2. [X] Specification having 30 pages(s) and including the following:
   - a. [X] Descriptive title of the invention
   - b. [ ] Cross references to related applications *(if applicable)*
   - c. [ ] Statement regarding Federally-sponsored research/development *(if applicable)*
   - d. [ ] Reference to microfiche appendix *(if applicable)*
   - e. [X] Background of the invention
   - f. [X] Brief summary of the invention
   - g. [X] Brief description of the drawings *(if drawings filed)*
   - h. [X] Detailed description
   - i. [X] Claims as classified below
   - j. [X] Abstract of the disclosure

Application Elements (continued)

3. [X] Drawing(s) *(when necessary as prescribed by 35 U.S.C. 113)*

   [ ] Formal   [X] Informal   Number of sheets: 3

4. [X] Oath or Declaration

   a. [X] Newly executed (original or copy)   [ ] Unexecuted

   b. [ ] Copy from a prior application (37 C.F.R. 1.63(d) *(for continuation/divisional applications only)*

   c. [ ] With Power of Attorney   [X] Without Power of Attorney

5. [ ] Incorporation by reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Computer program in microfiche

7. [ ] Genetic sequence submission *(if applicable, all must be included)*

   a. [ ] Paper copy

   b. [ ] Computer readable copy

   c. [ ] Statement verifying identical paper and computer readable copies

Accompanying Application

8. [X] Assignment papers *(cover sheet & document(s))*

9. [ ] 37 C.F.R. 3.73(b) statement *(when there is an assignee)*

10. [ ] English translation document *(if applicable)*

11. [ ] Information Disclosure Statement/PTO-1449   [ ] Copies of IDS citations

12. [ ] Preliminary Amendment

13. [X] Acknowledgment postcard

14. [ ] Certified copy of priority document(s) *(if foreign priority is claimed)*

15. [ ] Certificate of Mailing

    [ ] First Class   [ ] Express Mail (Label No.: ____________________)

16. [ ] Small Entity statement(s) -- # submitted ____________ *(if Small Entity status claimed)*

Accompanying Application (continued)

17. ☐ Additional enclosures *(please identify below):*

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

☒ Large Entity ☐ Small Entity

CLAIMS AS FILED					
For	**# Filed**	**# Allowed**	**# Extra**	**Rate**	**Fee**
Total Claims	96	- 20 =	76	x $18.00	$1,368.00
Independent Claims	7	- 3 =	4	x $78.00	$312.00
Multiple Dependent Claims (check if applicable) ☐					
Other Fees (specify purpose): Recordation Form Cover Sheet					$40.00
				BASIC FEE	$690.00
				TOTAL FILING FEE	$2,410.00

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☐ Charge the amount of _____ as filing fee.

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Dated: August 31, 2000

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MAGNETIC SHIELDING FOR INTEGRATED CIRCUITS

FIELD OF THE INVENTION

The present invention relates to a method and apparatus for shielding electromagnetic integrated circuits from external magnetic fields.

BACKGROUND OF THE INVENTION

In conventional packaging techniques, an integrated circuit chip or die is first attached to a carrier and then contacts of both the die and the carrier are electrically connected. One such packaged device, called a flip-chip device, requires a semiconductor chip to be flipped and bonded with a carrier, so that contacts of the chip directly bond to contacts of the carrier. Thus, both die bonding and interconnection are simultaneously accomplished.

A conventional bond flip-chip device 10 including an integrated circuit chip or die 30 and a flip-chip carrier 20 is illustrated in Figure 1. The flip-chip carrier 20 is fabricated from a substrate 12, an insulating layer 14, a plurality of conductive traces 15 (Figure 2) and an elastomeric layer 16. The conductive traces 15 may be located within or on the insulating layer 14 in a variety of ways, for example, by building up the conductive traces 15 on the insulating layer 14 through electrolytic deposition.

The conductive traces 15 (Figure 2) are each electrically connected to a solder ball 28 through an inset (not shown) in the substrate 12. Although a single solder ball 28 is shown in Figure 1, it must be understood that any number of solder balls 28 may be employed, as the solder balls 28 are used to mount the flip-chip device 10 to a circuit board or other electrical structure.

The die 30 is shown in dotted line above the flip-chip carrier 20. In use, the die 30 is positioned on the elastomeric material 16 of the flip-chip carrier 20. The flip-chip carrier 20 is electrically connected with the die 30 by way of suitable conductive connecting structures, such as, for example, solder balls 24 positioned within a gap 21 of the flip-chip carrier 20. The solder balls 24 are in electrical connection with respective conductive traces 15 and with suitable contacts on the die 30.

Recently, very-high density magnetic memories, such as magnetic random access memories (MRAMs), have been proposed to be integrated with CMOS circuits. This integration has also complicated the packaging of such devices, as the packaging must have a longer lifetime, better electrical performance, as well as more efficient heat dissipation.

A typical multilayer-film MRAM includes a plurality of bit or digit lines intersected by a plurality of word lines. At each intersection, layers of ferromagnetic film separated by a non-magnetic film are interposed between the corresponding bit line and word line to form a memory cell. When in use, an MRAM cell stores information as digital bits, the logic value of which depends on the states of

magnetization of the thin magnetic multilayer films forming each memory cell. As such, the MRAM cell has two stable magnetic configurations, high resistance representing, for example, a logic state 0 and low resistance representing, for example, a logic state 1. The magnetization configurations of the MRAMs depend in turn on the magnetization vectors which are oriented as a result of electromagnetic fields applied to the memory cells. The electromagnetic fields used to read and write data are generated by associated CMOS circuitry. However, stray magnetic fields, which are generated external to the MRAM, may cause errors in memory cell operation when they have sufficient magnitude.

Very high-density MRAMs are particularly sensitive to stray magnetic fields mainly because the minuscule MRAM cells require relatively low magnetic fields for read/write operations which, in turn, depend upon the switching or sensing of the magnetic vectors. These magnetic vectors are, in turn, easily affected and have the magnetic orientation changed by such external stray magnetic fields.

To diminish the negative effects of the stray magnetic fields and to avoid sensitivity of MRAM devices to stray magnetic fields, the semiconductor industry could produce memory cells requiring higher switching electromagnetic fields than a stray field which the memory cells would typically encounter. However, the current requirements for operating such memory cells is greatly increased because higher internal fields necessitate more current. Thus, the reliability and scalability of such high current devices decrease accordingly, and the use of MRAMs which may be affected by stray magnetic fields becomes undesirable.

Accordingly, there is a need for an improved magnetic memory packaging structure and a method of forming it, which shield against external magnetic fields and which permit use of lower power levels for circuit operations. There is also a need for a flip-chip packaging device for mounting a magnetic random access memory IC chip which reduces the effects of external magnetic fields on internal memory cell structures and operations. There is further a need for minimizing the cost of a packaging which shields a magnetic random access memory IC chip from external magnetic fields.

SUMMARY OF THE INVENTION

The present invention provides a method for fabricating magnetically shielded electromagnetic integrated circuit structures, such as MRAM structures. The present invention employs one or more magnetic shields which are incorporated either on an integrated circuit chip which contains electromagnetic structures, or in a flip-chip packaging device, or in both. In one exemplary embodiment of the invention, the electromagnetic shield is formed as one or more layers of magnetic field shielding material incorporated on the integrated circuit chip or in a flip-chip carrier, or both. In another exemplary embodiment, a printed circuit board supporting the flip-chip packaging may also include shielding material.

These and other features and advantages of the invention will be more clearly apparent from the following detailed description which is provided in connection with accompanying drawings and which illustrates exemplary embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a perspective view of a conventional flip-chip device.

Figure 2 is a top view of the conventional flip-chip device of Figure 1.

Figure 3 is a perspective view of an integrated circuit package assembly in accordance with a first exemplary embodiment of the present invention.

Figure 4 is a side view of the package assembly of Figure 3.

Figure 5 is a side view of the package assembly of Figure 3 and in accordance with a second exemplary embodiment of the present invention.

Figure 6 is a side view of the package assembly of Figure 3 and in accordance with a third exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description, reference is made to various specific embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural and electrical changes may be made without departing from the spirit or scope of the present invention.

Referring now to the drawings, where like elements are designated by like reference numerals, Figures 3-6 illustrate exemplary embodiments of the present invention. Figure 3 depicts an integrated circuit (IC) package assembly 100 at an intermediate stage of processing. A semiconductor chip or die 300 includes an array of internal electromagnetic structures, such as MRAM cells and access circuitry, and is shown in dotted line above a flip-chip carrier 200.

The flip-chip carrier 200 is fabricated from a substrate 120, an insulating layer 140, a plurality of conductive traces (not shown) and an elastomeric layer 160. The substrate 120 is typically formed of a material with high mechanical stability at high temperature. The substrate 120 may be a flexible tape such as, for example, a polyimide tape. Two commercially available polyimide tapes, KAPTON® from E. I. DuPont Nemours and Company and UPILEX® from Ube Industries, Ltd., can be employed to form the substrate 120. The elastomeric layer 160 may be formed of a silicone or a silicone-modified epoxy.

The conductive traces may be located within or on the insulating layer 140 in a variety of ways. One way, which is an addition method, is to build up the conductive traces on the insulating layer 140 through electrolytic deposition. The electrolytic deposition may be accomplished with a mask or, if performed without a mask, a subsequent etching step may be employed to create the conductive traces. Other suitable methods include sputter coating and laminating a sheet of conductive material, such as copper, and etching away excess copper to form the traces.

The conductive traces are each electrically connected to solder balls 280 through an inset (not shown) in the substrate 120. The solder balls 280 are used to mount the flip-chip device carrier 200 with the chip 300 to a circuit board or other electrical structure, as it will be described in more detail below.

As shown in Figure 3, the chip 300, including magnetic memory structures such as MRAM cells, is shown in dotted line above the flip-chip carrier 200. In use, the chip 300 is positioned on the elastomeric material 160 of the flip-chip carrier 200, as illustrated in Figure 4. As known in the art, the flip-chip carrier 200 is electrically connected with the chip 300 by way of suitable conductive connecting structures, such as, for example, solder balls 240 positioned within a gap 210 of the carrier 200. The solder balls 240 are in electrical connection with respective conductive traces 150 (not shown) and with suitable contacts on the chip 300.

Referring now to Figures 3-4, a first magnetic shielding layer 110 is provided for shielding the chip 300 from external magnetic field disturbances. According to a first exemplary embodiment of the present invention, the first magnetic shielding layer 110 is formed on the back surface of the semiconductor chip 300, that is the surface that is opposite to a front surface of the semiconductor chip 300 or the surface that directly contacts the flip-chip carrier 200.

The first magnetic shielding layer 110 comprises a magnetic shielding material which can be formed, for example, of an electrically non-conductive material with permeability higher than that of air or silicon. As such, the preferred choice for the magnetic shielding material is a non-conductive magnetic oxide, for

example, a ferrite such as MFe_2O_4, wherein M = Mn, Fe, Co, Ni, Cu, or Mg, among others. Manganites, chromites and cobaltites may be used also, depending on the device characteristics and specific processing requirements. Further, the magnetic shielding material may be also composed of conductive magnetic particles, for example nickel, iron or cobalt particles, which are incorporated into a non-conductive base material, such as a glass sealing alloy or a polyimide. Alternatively, the magnetic shielding material may be formed of a film or layer of conductive magnetic material, such as nickel, cobalt, iron, Permalloy, or Mumetal, among others.

Next, as illustrated in Figure 4, the flip-chip carrier 200 with the attached chip 300 is further attached to a portion of a printed circuit board 400 by surface mounting, for example. This way, the flip-chip carrier 200 is mounted flat on the printed circuit board 400 and contacts the printed circuit board 400 through the solder balls 280, eliminating the need for holes through the printed circuit board.

As shown in Figure 4, a flat layer 111 of magnetic shielding material may be embedded within the printed circuit board, which can be otherwise formed of a resin compound, for example, or other known printed circuit board material. In this case, the magnetic memory structures of the chip 300 are first shielded by the first magnetic shielding layer 110 and further shielded by the flat layer 111 of the printed circuit board 400 for maximum protection from external stray magnetic fields.

Although Figure 4 shows the magnetic shielding material in the form of layer 110 on the backside of chip 300 and as layer 111 embedded within the printed

circuit board 400, it is also possible to apply a layer of shielding material on the bottom surface of the printed circuit board 400 instead. For example, Figure 5 illustrates another exemplary embodiment of the present invention, in which a bottom magnetic shielding layer 112 is formed on the bottom surface of the printed circuit board 400, together with the flat layer 111 embedded within the printed circuit board 400.

The preferred material for the bottom magnetic shielding layer 112 is a conductive Mumetal alloy comprising, for example, approximately 77% nickel (Ni), 4.8% copper (Cu), 1.5% chromium (Cr) and 14.9% iron (Fe), as well as conductive magnetic particles, such as nickel or iron particles, incorporated into a molding material, for example a glass sealing alloy or a commercially available mold compound. However, non-conductive magnetic oxide, for example a ferrite such as MFe_2O_4, wherein M = Mn, Fe, Co, Ni, Cu, or Mg, among others, may be used also, as well as manganites, chromites and cobaltites, depending on the device characteristics and processing requirements.

In yet a third embodiment of the present invention, another magnetic shielding layer 113 is formed of a magnetic shielding material as part of the flip-chip carrier 200, as shown in Figure 6. The magnetic shielding layer 113 is formed between the substrate 120 and the insulating layer 140 to further protect the MRAM devices from external magnetic fields and to complete the fabrication of an IC package assembly 102 (Figure 6). The magnetic shielding material may be different than, or similar to, the magnetic shielding materials for layers 110, 111 and

112. Appropriate conductive vias, insulated from magnetic shielding layer 113, are formed through layer 113. Again, the magnetic shielding material may be preferably a non-conductive magnetic oxide, for example a ferrite such as MFe_2O_4, wherein M = Mn, Fe, Co, Ni, Cu, or Mg, among others, or a manganite, chromite or cobaltite. Further, the magnetic shielding material may be also composed of magnetic particles, for example nickel, iron or cobalt particles, which are incorporated into a base material such as a glass sealing alloy or a commercially available mold compound. Since nickel is conductive, however, the concentration of nickel particles in the glass alloy should be low enough so that the shielding material does not form a continuous conductor, unless appropriate conductive vias electrically insulated from the magnetic layer are used.

Although the exemplary embodiments described above refer to specific magnetic shielding materials, it must be understood that the invention is not limited to the materials described above, and other magnetic shielding materials, such as ferromagnetics like nickel-iron (Permalloy), cobalt-nickel-iron, nickel or iron may be used also.

In addition, the magnetic shielding material forming the various shielding layers described above may also comprise a mold compound, such as a plastic compound, with conductive magnetic particles therein. For example, conductive magnetic particles of, for example, nickel, iron, and/or cobalt, may be suspended in a matrix material, such as a plastic compound, at a concentration that does not allow the particles to touch each others. Alternatively, the magnetic shielding material

may comprise a molding material including non-conductive particles of, for example, non-conductive magnetic oxides and/or Mumetal alloys. Mumetal alloys may comprise, for example, approximately 77% nickel (Ni), 4.8% copper (Cu), 1.5% chromium (Cr) and 14.9% iron (Fe).

Further, although the exemplary embodiments described above refer to specific locations where the shielding material is applied to a chip, it is also possible to apply the shielding material in other locations. For example, it is also possible to apply a layer of shielding material on both the top and bottom surfaces of the printed circuit board 400, or on the top and bottom surfaces together with a shielding material embedded within the printed circuit board. Further, a plurality of layers of material could be employed for shielding the magnetic memories structures, one on each side of chip 300, or layers of the same or different shielding materials which overlap each other may be used on one or both sides of chip 300, flip-chip carrier 200 and/or circuit printed board 400. In addition, the specific shape of the shielding material is not limited to that shown in Figures 3-6 and other shapes, configurations, or geometries may be employed. Also, the chip 300 and associated flip-chip carrier 100 may be encapsulated in a flip-chip package which is mountable through solder balls 180 to a printed circuit board.

The present invention is thus not limited to the details of the illustrated embodiments and the above description and drawings are only to be considered illustrative of exemplary embodiments which achieve the features and advantages of the present invention. Modifications and substitutions to specific process conditions

and structures can be made without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

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What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An integrated circuit structure comprising:

at least one integrated circuit chip containing structures which may be affected by external magnetic fields, said integrated circuit chip having a front surface and a back surface, said front surface being supported by a chip carrier; and

a magnetic field shielding material in contact with said back surface of said chip.

2. The structure of claim 1, wherein said shielding material is in the form of a first layer of said magnetic field shielding material on said back surface.

3. The structure of claim 1, wherein said shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

4. The structure of claim 3, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

5. The structure of claim 3, wherein said magnetic material comprises a material which includes conductive particles.

6. The structure of claim 5, wherein said magnetic material comprises a material which includes nickel particles.

7. The structure of claim 5, wherein said magnetic material comprises a material which includes iron particles.

8. The structure of claim 5, wherein said magnetic material comprises a material which includes cobalt particles.

9. The structure of claim 1, wherein said chip contains a magnetic memory structure.

10. The structure of claim 9, wherein said magnetic memory structure is a magnetic random access memory device.

11. The structure of claim 1, wherein said chip carrier is a flip-chip carrier.

12. The structure of claim 11, wherein said flip-chip carrier further comprises a second magnetic field shielding layer.

13. The structure of claim 12, wherein said second magnetic field shielding layer comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

14. The structure of claim 13, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

15. The structure of claim 13, wherein said magnetic material comprises a material which includes conductive particles.

16. The structure of claim 15, wherein said magnetic material comprises a material which includes nickel particles.

17. The structure of claim 15, wherein said magnetic material comprises a material which includes cobalt particles.

18. The structure of claim 15, wherein said magnetic material comprises a material which includes iron particles.

19. The structure of claim 11 further comprising a printed circuit board having an upper surface and a bottom surface, said upper surface supporting said flip-chip carrier.

20. The structure of claim 19, wherein said printed circuit board further comprises a third magnetic field shielding layer.

21. The structure of claim 20, wherein said third magnetic field shielding layer is located on said upper surface of said printed circuit board.

22. The structure of claim 20, wherein said third magnetic field shielding layer is located on said bottom surface of said printed circuit board.

23. The structure of claim 20, wherein said third magnetic field shielding layer is embedded within said printed circuit board.

24. The structure of claim 20, wherein said third magnetic field shielding layer comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

25. The structure of claim 20, wherein said magnetic material comprises a material which includes conductive particles.

26. The structure of claim 25, wherein said magnetic material comprises a material which includes nickel particles.

27. The structure of claim 20, wherein said printed circuit board further comprises a fourth magnetic field shielding layer in contact with said bottom surface, said third magnetic field shielding layer being embedded within said printed circuit board.

28. The structure of claim 27, wherein each of said fourth and third magnetic field shielding layers comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

29. The structure of claim 28, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

30. The structure of claim 28, wherein said magnetic material comprises a material which includes conductive particles.

31. The structure of claim 30, wherein said magnetic material comprises a material which includes nickel particles.

32. An integrated circuit chip containing structures which may be affected by external magnetic fields, said chip comprising a magnetic field shielding material in contact with a surface of said chip.

33. The integrated circuit chip of claim 32, wherein said magnetic field shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

34. The integrated circuit chip of claim 33, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

35. The integrated circuit chip of claim 33, wherein said magnetic material comprises a material which includes conductive particles.

36. The integrated circuit chip of claim 35, wherein said magnetic material comprises a material which includes nickel particles.

37. The integrated circuit chip of claim 35, wherein said magnetic material comprises a material which includes iron particles.

38. The integrated circuit chip of claim 35, wherein said magnetic material comprises a material which includes cobalt particles.

39. The integrated circuit chip of claim 32, wherein said chip contains a magnetic memory structure.

40. The integrated circuit chip of claim 39, wherein said magnetic memory structure is a magnetic random access memory device.

41. A chip carrier for supporting an integrated circuit chip containing structures which may be affected by external magnetic fields, said chip carrier comprising:

a substrate having a top surface and a bottom surface supporting first conductive elements;

an insulating layer over said top surface of said substrate, said insulating layer including a plurality of conductive traces which are connected to said first conductive elements;

a chip support surface over said insulating layer;

second conductive elements for connection between contacts of a chip supported on said support surface and said conductive traces; and

a layer of magnetic field shielding material.

42. The chip carrier of claim 41, wherein said magnetic field shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

43. The chip carrier of claim 42, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

44. The chip carrier of claim 42, wherein said magnetic material comprises a material which includes conductive particles.

45. The chip carrier of claim 44, wherein said magnetic material comprises a material which includes nickel particles.

46. The chip carrier of claim 44, wherein said magnetic material comprises a material which includes iron particles.

47. The chip carrier of claim 44, wherein said magnetic material comprises a material which includes cobalt particles.

48. The chip carrier of claim 41, wherein said layer of magnetic field shielding material is located in between said top surface of said substrate and said insulating layer.

49. The chip carrier of claim 41, wherein said layer of magnetic field shielding material is located on said bottom surface of said substrate.

50. The chip carrier of claim 41, wherein said layer of magnetic field shielding material is located over said top surface of said insulating layer.

51. The chip carrier of claim 41, wherein said integrated circuit chip contains a magnetic memory structure.

52. The chip carrier of claim 51, wherein said magnetic memory structure is a magnetic random access memory device.

53. A printed circuit board comprising:

a support body having a top surface and a bottom surface, said top surface being in contact with a flip-chip carrier; and

at least one layer of a magnetic field shielding material.

54. The printed circuit board of claim 53, wherein said layer of magnetic field shielding material is located on said top surface of said support body.

55. The printed circuit board of claim 53, wherein said layer of magnetic field shielding material is located on said bottom surface of said support body.

56. The printed circuit board of claim 53, wherein said layer of magnetic field shielding material is located on both said top and bottom surfaces of said support body.

57. The printed circuit board of claim 53, wherein said layer of magnetic field shielding material is embedded within said support body.

58. The printed circuit board of claim 53, wherein said layer of magnetic field shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

59. The printed circuit board of claim 53, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

60. The printed circuit board of claim 53, wherein said magnetic material comprises a material which includes conductive particles.

61. The printed circuit board of claim 60, wherein said conductive particles are selected from the group consisting of nickel particles, iron particles, and cobalt particles.

62. The printed circuit board of claim 53, further comprising an integrated circuit chip which contains a magnetic memory structure mounted on said top surface of said support body.

63. The circuit printed board of claim 62, wherein said magnetic memory structure is a magnetic random access memory device.

64. An integrated circuit structure comprising:

a die electrically connected to a die carrier, said die being in contact with a first layer of magnetic field shielding material, said die further comprising a magnetic random access memory device; and

a printed circuit board electrically connected to said die carrier, said printed circuit board being in contact with a second layer of magnetic field shielding material.

65. The integrated circuit structure of claim 64, wherein said die carrier comprises a third layer of magnetic field shielding material.

66. The integrated circuit structure of claim 65, wherein each of said first, second and third layers of magnetic field shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

67. The integrated circuit structure of claim 66, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

68. The integrated circuit structure of claim 66, wherein said magnetic material comprises a material which includes conductive particles.

69. The integrated circuit structure of claim 68, wherein said conductive particles are selected from the group consisting of nickel particles, iron particles, and cobalt particles.

70. A method of packaging a semiconductor device comprising:

electrically coupling a die carrier to a first surface of a die, said first surface being opposite to a second surface of said die; and

contacting said second surface of said die with a first layer of magnetic field shielding material which shields said die from external magnetic fields.

71. The method of claim 70 further comprising the act of electrically coupling said die carrier to a printed circuit board which has a second layer of magnetic field shielding material.

72. The method of claim 71, wherein said act of contacting said printed circuit board with said second layer of magnetic field shielding material wherein said second layer of magnetic field shielding material is formed on a surface of said printed circuit board.

73. The method of claim 72, wherein said second layer of magnetic field shielding material is formed on a top surface of said printed circuit board.

74. The method of claim 72, wherein said second layer of magnetic field shielding material is formed on a bottom surface of said printed circuit board.

75. The method of claim 72, wherein said second layer of magnetic field shielding material is embedded within said printed circuit board.

76. The method of claim 72, wherein said second layer of magnetic field shielding material is formed on both a bottom surface and a top surface of said printed circuit board.

77. The method of claim 70, wherein said semiconductor device is a magnetic memory device.

78. The method of claim 77, wherein said magnetic memory device is a magnetic random access memory device.

79. The method of claim 70, wherein said first layer of magnetic field shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

80. The method of claim 79, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

81. The method of claim 79, wherein said magnetic material comprises a material which includes conductive particles.

82. The method of claim 81, wherein said conductive particles are selected from the group consisting of nickel particles, iron particles, and cobalt particles.

83. The method of claim 71, wherein said second layer of magnetic field shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

84. The method of claim 83, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

85. The method of claim 83, wherein said magnetic material comprises a material which includes conductive particles.

86. The method of claim 85, wherein said magnetic material comprises a material which includes nickel particles.

87. A method of forming a chip carrier for supporting an integrated circuit chip containing structures which may be affected by external magnetic fields, said method comprising:

forming an insulating layer over a first surface of a substrate;

providing a support surface for said integrated circuit chip; and

providing a layer of magnetic field shielding material which shields said integrated circuit chip from external magnetic fields.

88. The method of claim 87, wherein said layer of magnetic field shielding material is formed between said insulating layer and said first surface of said substrate.

89. The method of claim 87, wherein said layer of magnetic field shielding material is embedded within said substrate.

90. The method of claim 87, wherein said layer of magnetic field shielding material is formed on both a bottom surface and a top surface of said printed circuit board.

91. The method of claim 87, wherein said semiconductor device is a magnetic memory device.

92. The method of claim 91, wherein said magnetic memory device is a magnetic random access memory device.

93. The method of claim 87, wherein said layer of magnetic field shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

94. The method of claim 93, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

95. The method of claim 93, wherein said magnetic material comprises a material which includes conductive particles.

96. The method of claim 95, wherein said conductive particles are selected from the group consisting of nickel particles, iron particles, and cobalt particles.

ABSTRACT

A method and apparatus which provide one or more electromagnetic shield layers for integrated circuit chips containing electromagnetic circuit elements are disclosed. The shield layers may be in contact with the integrated circuit chip, including magnetic memory structures such as MRAMs, or in a flip-chip carrier, or both. A printed circuit board which supports the chip may also have one or more shield layers.

Figure 1

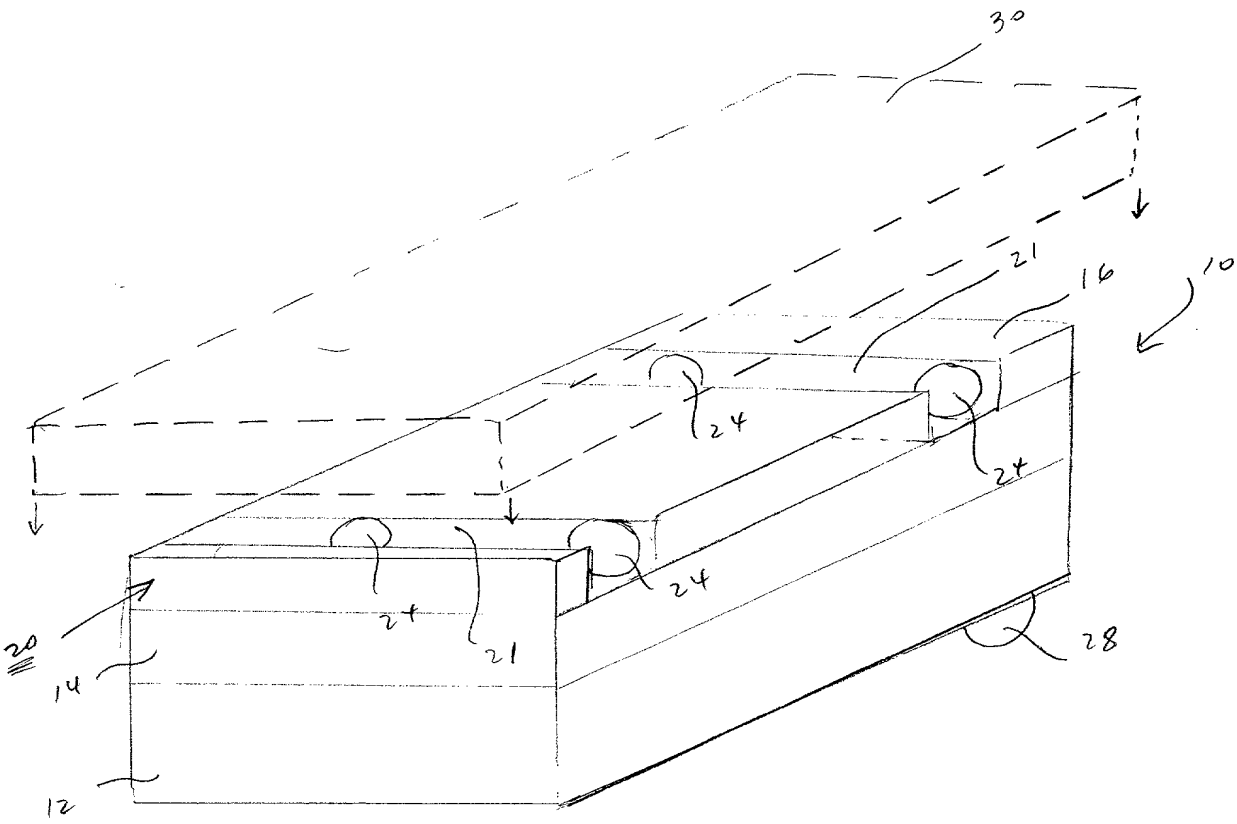


Figure 2

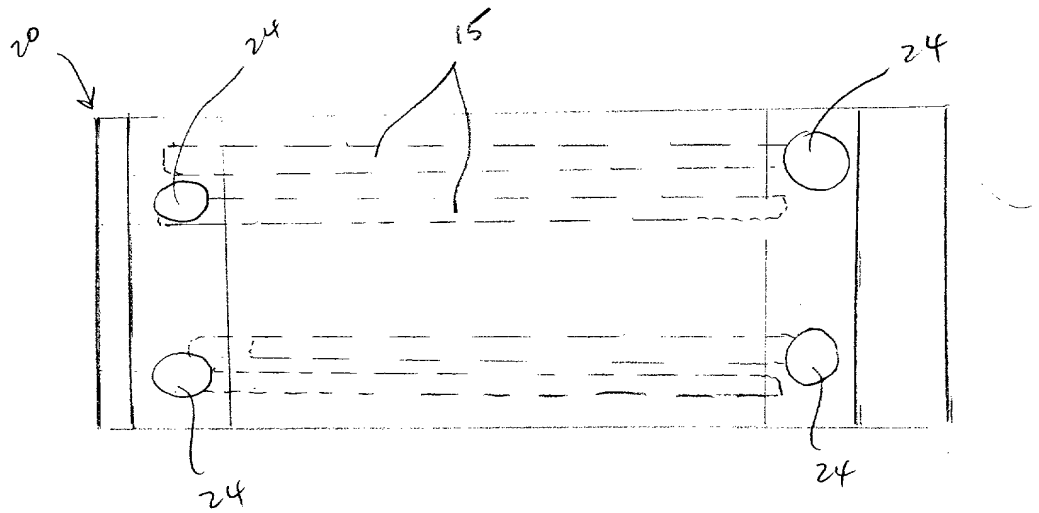


Figure 3

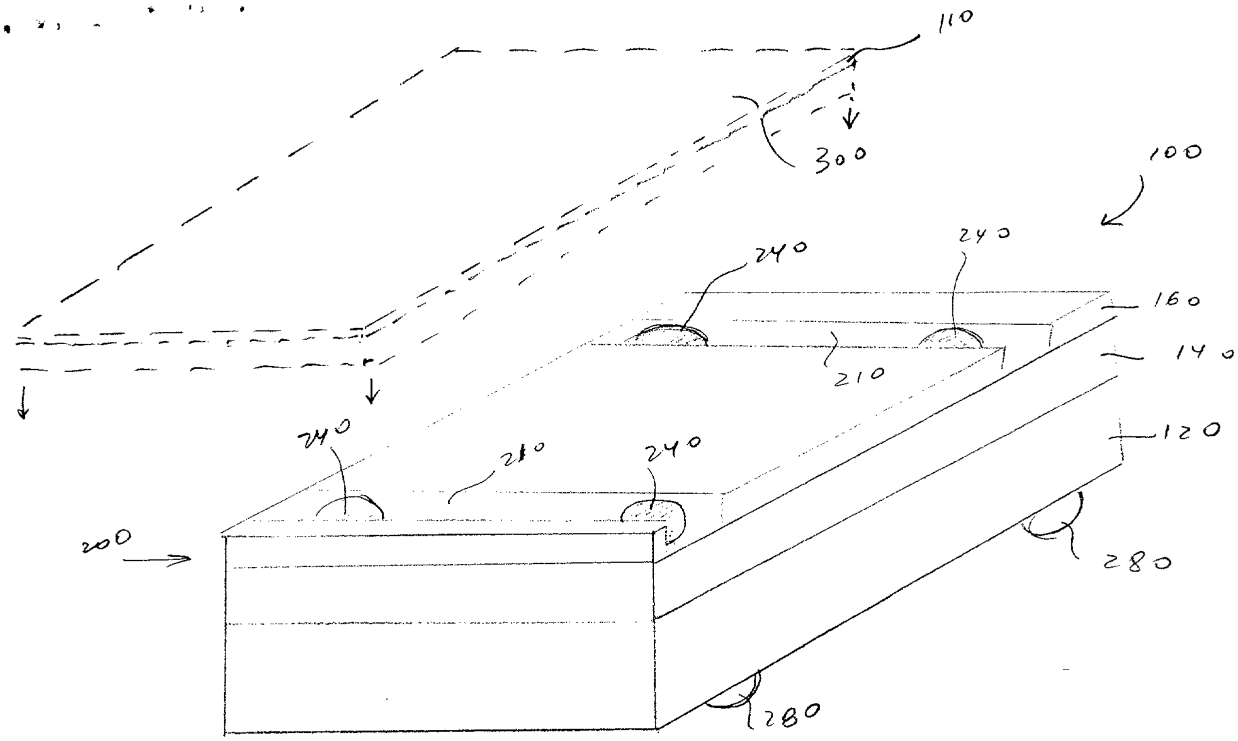


Figure 4

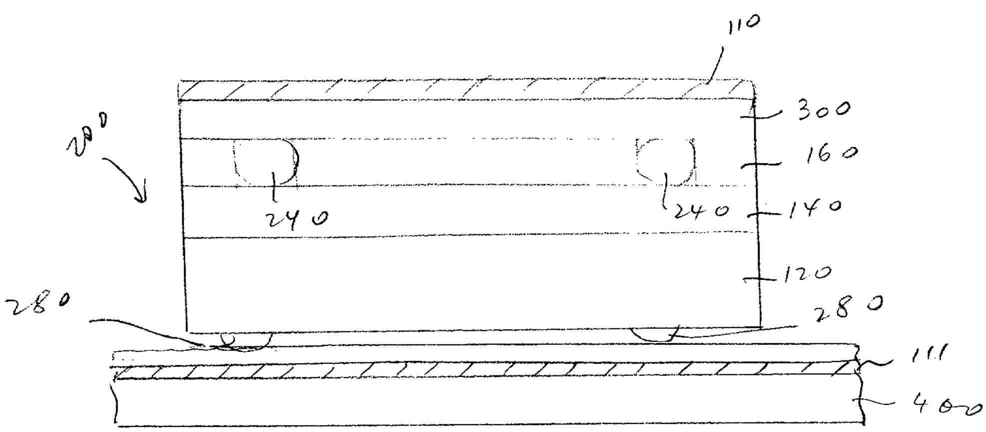


Figure 5

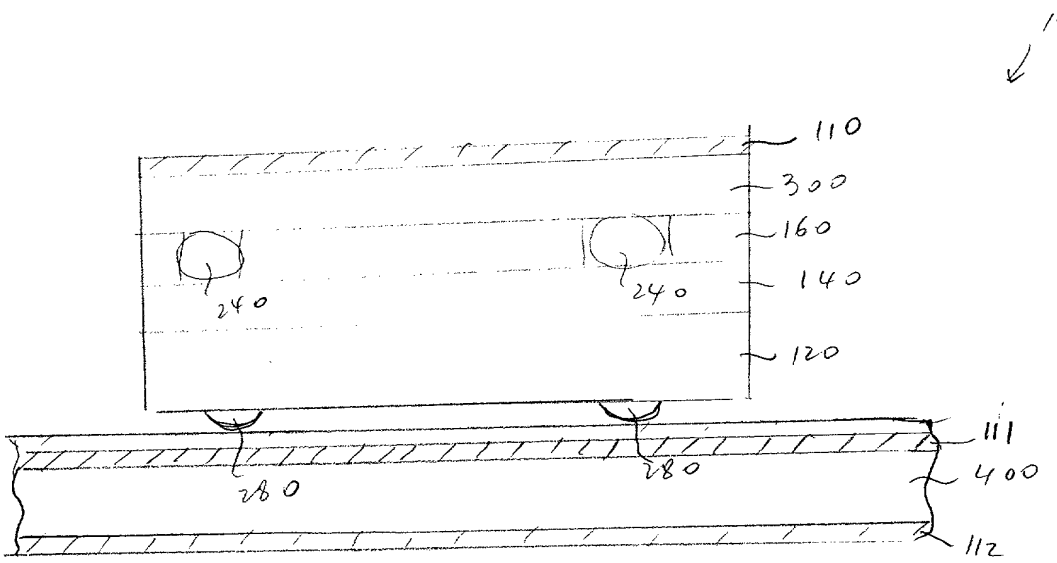
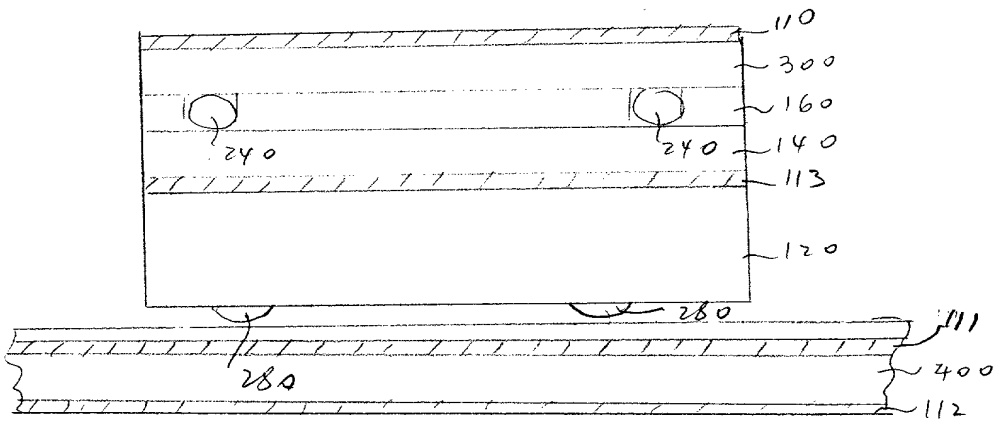


Figure 6



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MAGNETIC SHIELDING FOR INTEGRATED CIRCUITS

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the

subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street NW, Washington, DC 20037-1526. Telephone calls should be made to (202) 785-9700.

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